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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,378	11/25/2003	Nobuyuki Sekikawa	492322001810	4282

7590 02/24/2005

Barry E. Bretschneider
Morrison & Foerster LLP
Suite 300
20001650 Tysons Boulevard
McLean, VA 22102

EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,378	NOBUYUKI SEKIKAWA	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/13/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *6-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/925,628.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/13/04 & 11/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), claiming priority from U.S. Serial No. 09/925,628 filed on August 21, 2001 which itself claims priority from Japanese Patent Application No. 2000-242617 filed on August 10, 2000 which papers have been placed of record in the file.

Divisional Prosecution Application

The request filed on 11/25/2003 for a Divisional Prosecution Application (Div.) based on parent Application No. 09/925628 is acceptable and Div. has been established. An action on the Div. follows.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled on November 25, 2003 and July 13, 2004 .

The references on PTO 1499 submitted on November 25, 2003 and July 13, 2004 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 11 / 25/2003.

Therefore claims 6 to 9 as amended by the preliminary amendment and claims 10-11 as presently newly added are currently pending in the Application.

Claim Rejections - 35 USC § 103

.The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 to 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi (U.S. Patent No. 5,937,909, herein after Moslehi) in view of Araki (U.S. Patent No. 5,882,994, herein after Araki).(both cited in the parent case and included by the Applicants in their PTO-1449 of the present case).

With respect to claim 6 Moslehi describes a method of manufacturing an insulated gate semiconductor device comprising: forming a first gate oxide on a semiconductor substrate of a first conductivity type; (Moslehi figure 2 # 48 over 38, col. 11 lines 23-25) forming a first silicon layer on the first gate oxide film ; (Moslehi fig. 3 # 50 over 48, col.11 line 35) forming an oxidation protection film having a predetermined pattern on the first silicon layer ; (Moslehi figure 3 # 52 over 50 , col. 11 line20) forming a field

oxidation film (Moslehi figure 3 #42) and a second gate oxide film through selective oxidation by using the oxidation protection film as a mask.

Moslehi does not specifically describe a second gate oxide film through selective oxidation by using the oxidation protection film as a mask.

However, Araki, a patent from the same filed of endeavor, describes in figures 6-7 and col. 4 lines 51-65, etc. describes a second ONO insulation film to form insulators with enhanced insulation characteristics and charge storage characteristics.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Araki's second insulating ONO layer in Moslehi's device to form insulators with enhanced insulation characteristics and charge storage characteristics (Arkai col. 1 lines 53-56) the second gate oxide film being in contact with the first gate oxide film; (Araki figure 7 106 in contact with 105).

The remaining limitations of claim 1 are :

forming a second silicon layer covering the first silicon laver remaining after the selective oxidation the second gate oxide film and the field oxidation film after removing the oxidation protection film; (Araki fig. 8 # 107, col. 4 line 56-58 col. 14 line 16) isolating a portion of the second silicon layer by etching so that the isolated portion of the second silicon layer covers at least part of the second gate oxide film and a portion of the remaining first silicon laver; (Araki col. 4 lines 56-65) forming a source layer or a drain layer which is of a second conductivity type. (Moslehi figure 3 col. 10 lines 50-55).

With respect to claim 7 Moslehi describes a method of manufacturing an insulated gate semiconductor device comprising: forming a low impurity concentration source layer and a low impurity concentration drain layer which are of a second conductivity type(Moslehi figure 4 # 58, col.12 lines 25-30) in a semiconductor substrate of a first conductivity type; (Moslehi figure 4 # 38, col. 10 lines 50-55) forming a first gate oxide film on the semiconductor substrate; (Moslehi figure 2 # 48, col. 11 lines 23-25) forming a first silicon layer on the first gate oxide film (Moslehi fig. 3 #50 over 48, col.11 line 35) forming an oxidation protection film having a predetermined pattern on the first Silicon layer (Moslehi fig. 3 #52, col.11 line 20) forming a field oxidation film (Moslehi fig. 4 #42, col. 10 line 59)

Moslehi does not specifically describe second gate oxide through selective oxidation by using the oxidation protection film as a mask the second gate oxide being in contact with the first gate oxide film.

However, Araki, a patent from the same filed of endeavor, describes in figures 6- 7 and col. 4 lines 51-65, etc. describes a second ONO insulation film to form insulators with enhanced insulation characteristics and charge storage characteristics.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Araki's second insulating ONO layer in Moslehi's device to form insulators with enhanced insulation characteristics and charge storage characteristics (Arkai col. 1 lines 53-56) the second gate oxide film being in contact with the first gate oxide film; (Araki figure 7 106 in contact with 105).

The remaining limitations of claim 7 are :

isolating a portion of the second silicon layer by etching so that the isolated portion of the second silicon laver is positioned between the low impurity concentration source and drain layers and covers the remaining first silicon laver and at least part of the second gate oxide; and forming ; (Araki col. 4 lines 56-65) light impurity concentration source layer of the second conductivity type in the low impurity concentration source layer and forming a high impurity concentration drain layer of the second conductivity type in the low concentration drain layer. (Moslehi figure 7, col. 13 lines 49 to 55).

With respect to claims 8 and 10 Moslehi describes the method of manufacturing an insulated gate semiconductor device of claim 7, wherein the first and second silicon layers comprise polysilicon or amorphous silicon. (Moslehi col.11 lines 37-40).

With respect to claims 9 and 11 Moslehi describes the method of manufacturing an insulated gate semiconductor device of claim 7, wherein the oxidation protection layer comprises silicon nitride. (col. 12 lines 20-25- layer 52 other than oxide col.11 lines 29-31- nitrided oxides, etc.,)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is ((571) 272 -1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

Feb. 19, 2005.